REMARKS

The present invention is a receiver and a method of data reception. In accordance with the invention, a memory 114, including an addressable storage array, stores a sequence of data samples contained in a time division multiplexed signal, as illustrated in Fig. 3. The time division multiplexed signal is from a plurality of channels in the incoming data sequence 202. Each successive data sample belongs to a channel different from a channel to which an immediately preceding data sample belongs. The memory outputs the stored data samples in a sequence of data groups equal in number to the number of channels, which in the example of Fig. 3, is five. Each data group has a plurality of samples, as illustrated in Fig. 3. The contents of the memory 114, which are read in as a sequence of data samples from different channels, are read out as a sequence of data groups, as illustrated in the bottom of Fig. 3. Thereafter a decoder, as exemplified by decoder 116 in Fig. 2, which is responsive to the sequence of data groups, decodes the data samples within the sequence of data groups and outputs the decoded data samples of the plurality of data groups from the plurality of channels.

This architecture has distinct advantages over the prior art of Fig. 1. As described in Applicant's specification with reference to Fig. 1, the prior art hardware identified by reference numeral 10 requires replication for each channel.

In contrast, the present invention has an exemplary architecture illustrated in Fig. 2, which utilizes only a single memory 114 and an inner decoder 116 to achieve decoding of data for the R channels of Fig. 1. The present invention requires substantially less hardware requirements than the prior art. See Applicant's

specification, beginning on page 17, line 9, for a discussion regarding the hardware reduction achieved by the present invention.

Claims 18, 19, 21, 22, 24, 25 and 27 stand rejected under 35 USC §112, second paragraph regarding the dependency of claim 18. Claim 18 has been amended to correct its dependency to claim 17, which overcomes the stated ground of rejection.

Claims 1 and 17 stand rejected under 35 USC §102 as being anticipated by U.S. Patent No. 5, 448,592 (Williams *et al.*). The Examiner reasons as follows:

> "10. Regarding claim 1, Williams et al. shows a receiver comprising: a memory (Williams fig. 11:26 'register') including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal (Williams et al. claim 13) from a plurality channels (Williams fig. 11:'16x8', '16x8') and outputs the stored data samples in a sequence of data groups (Williams fig. 11: '32x7', '33'x1 (implied)) with each data group containing a plurality of samples from one of the plurality of channels; and a decoder (Williams fig. 11:28), responsive to the data groups, which decodes the data samples within the data groups and outputs decoded data samples.
>
> 11. Regarding claim 17, the discussion for claim 1 applies."

This ground of rejection is traversed for the following reasons.

Claim 1 recites "a receiver comprising: a memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal from a plurality of channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs and outputs the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels with each data group containing a plurality of samples from one of the plurality of channels; and a decoder, responsive to the sequence of data groups, which decodes the data samples within the sequence of data groups and outputs decoded data samples of the plurality of data

groups from the plurality of channels" and claim 17 recites "a method of data reception comprising: receiving and storing a timed division multiplex signal containing a sequence of data samples from a plurality of channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs; outputting the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels, each data group containing a plurality of samples from one of the plurality of channels; decoding the data samples within the sequence of data groups, and outputting the decoded samples of the plurality of data groups from the plurality of channels." This subject matter is not taught by Williams et al.

Williams et al. disclose, in Fig. 10, a coder which produces output signal 16 which is demodulated by demodulator 20 of Fig. 11. The Examiner has relied upon Fig. 11 as anticipating claims 1 and 17. In order to properly understand Williams et al., it is necessary to analyze the data modulation of Fig. 10 to determine the nature of the signals being sent and how the transmitting signals are demodulated by Fig. 11 which the Examiner contends anticipates claims 1 and 17.

In Fig. 10, an input 1, which is data, is clocked into a sixty-four bit serial to parallel shift register 2. Every sixty-four bits of the input data are output as a parallel sixty-four bit word into register 4. From register 4, six bits are fed to coder 5 and twenty-six bits are fed to coder 6. Coder 5 implements a (32, 6, 16) Reed-Muller decoder and produces thirty-two bits a_{1j} and coder 6 is an (32, 26, 4) extended Hamming-coder which produces thirty-two bits a_{2j}. A remaining thirty-two bits a_{3j} are produced in an uncoded form, as shown in Fig. 9. See column 7, lines 31-50.

The ninety-six bits comprising a_{1j}, a_{2j}, and a_{3j} are fed to registers 7-12. See column 7, lines 51-63. The contents of the registers 7-12 are X and Y coordinates of sixteen symbols to be transmitted. A three-bit word representing the X coordinate of the symbol to be transmitted is output by registers 7-9 and a three-bit data word representing the Y coordinates is output by registers 10-12. See column 7, lines 63 through column 8, line 5.

The outputs from the registers 7-9 and 10-12 respectively modulate orthogonal carriers C_I and C_Q which are summed together in the output 16. See column 8, lines 6-19.

Fig. 11, as stated above, shows a corresponding demodulator for the modulator of Fig. 10. Column 8, line 53 through column 9, line 30 describe the decoding process which operates to load shift registers 24 and 25 with the X and Y coordinates, as described above with respect to Fig. 10. Bit outputs are packed into the shift registers 24 and 25 to define data fields of 16 x 8 bits which are, in turn, combined by shift register 26 into a data field of 32 x 8 bits. It is therefore seen that a sequence of X and Y coordinates are processed by shift registers 24, 25 and 26 to define a data field of 32 x 8 bits. Thereafter, the Reed-Muller decoder 28 outputs six data bits to register 30 with an additional twenty-six bits being decoded by extended Hamming decoder 32 which are also outputted to register 30. Finally, thirty-two uncoded bits are passed to unit 32, which adjusts the bits and inputs them to register 34. It is seen that the output from register 34 is sixty-four bits.

It is submitted that the foregoing operation of Williamson *et al.* does <u>not</u> correspond to the claimed sequence of data samples contained in a time division

multiplexed signal from a plurality of channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs. Furthermore, the above operation does not correspond to outputting stored data samples in a sequence of data groups equal in number to a number of the plurality of channels and, does not correspond to a decoder responsive to the sequence of data groups, which decodes the data samples within the sequence of data groups and outputs decoded data samples of the plurality of data groups from the plurality of channels as recited in claim 1 and as substantively recited in claim 17.

The Examiner relies upon claim 13, which recites "time division multiplex means, synchronized to the block timing means, for combining data input to the apparatus and additional information to produce the block of bits to be transmitted," as suggesting that the above sequence of Fig. 10 would be time division multiplexed. Apparently, this claimed subject matter may be readable upon column 15, line 8 through 23, or possibly some other portion of Williams et al. However, it is submitted that the recitation in claim 13 of time division multiplex means and further the teaching in the specification of multiplexing a secondary channel would not be understood by a person of ordinary skill in the art in combination with Figs. 10 and 11 to anticipate the subject matter of claims 1 and 17. If the Examiner persists in the stated ground of rejection, it is requested that he specifically point out how time division multiplexing would be performed in the data modulation of Fig. 10 and the data demodulation of Fig. 11, such that the subject matter of claims 1 and 17 would be readable on Fig. 11.

Claims 2-16 and 18-29 stand rejected under 35 USC §103 as being unpatentable over U.S. Patent No. 6,279,132 (Linsky et al.). The Examiner reasons as follows:

16. Regarding claim 2, Linsky shows the data samples comprising orthogonally encoded data (Linsky col. 2 last full paragraph); and the decoder is a biorthogonal inner code soft decision data decoder (Linsky: col. 6, lines 50 to 53). Linsky et al. also shows a receiver (Linsky fig. 2:213) comprising: a memory (Linsky et al. col. 1: line 64) including an addressable storage array which stores a sequence of data samples from a plurality channels and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; and a decoder (Linsky fig. 2:216), responsive to the data groups, which decodes the data samples within the data groups and outputs decoded data samples. What Linsky does not show is that the data samples are time division multiplexed. It would have been obvious to one skilled in the art at the time of the invention to modify Linsky to have TDM inputs because it is well known in the art that multiple access increases efficiency and one way of achieving multiple access is via time division multiplexing.

17. Regarding claim 3, claim 2 is discussed above. Linsky shows a receiver wherein the biorthogonal inner code soft decision data decoder is a Reed Muller decoder (Linsky: col. 4, lines 2-3, last full paragraph).

18. Regarding claim 4, claim 2 discussed above. Linsky shows a receiver wherein the orthogonally encoded data samples are QPSK encoded (Linsky: col. 3, third full paragraph).

19. Regarding claims 5 to 8, Linsky shows the receiver is contained in a satellite (Linsky: col. 3, fourth full paragraph).

20. Regarding claims 9 to 12, Linsky shows a channelizer (Linsky: fig. 213), which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth (Linsky fig. 1: 116, 117). What Linsky does not show is one of the output channels comprising the time division multiplexed signal. It would have been obvious to one skilled in the art at the time of the invention to modify Linsky to have TDM outputs because it is well known in the art that multiple access increases efficiency and one way of achieving multiple access is via time division multiplexing.

21. Regarding claims 13 to 16, it is inherent for the memory in Linsky et al. (Lindsky et al. col. 1: line 64) to comprise a write address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator. It is inherent since these are characteristic elements of a memory.

22. Regarding claims 18 to 29, the above discussion for claims 2-16 apply."

This ground of rejection is traversed for the following reasons:

The Examiner's rejection is predicated upon the system of Fig. 2 of Linsky et al. However, Linsky et al. describes only very briefly in column 4, lines 8 through 19, the system of Fig. 2. Furthermore, the operation of the receiver of Fig. 2 is described in column 6, line 32 through column 7, line 24. None of these portions of Linsky et al. describe the sequence of signal processing recited in claims 1 and 17 as described above. Moreover, a person of ordinary skill in the art would not be led to modify Linsky et al. to arrive at the subject matter of claims 1 and 17.

The Examiner in section 16 quoted above seems to place significant reliance upon the fact that it is obvious to utilize time division multiplexing and if time division multiplexing were used with the receiver of Fig. 2, that the subject matter of claims 2-16 and 18-29 would be achieved. First, it is submitted that such reasoning is based upon impermissible hindsight. The Examiner has not suggested how time division multiplexing would be utilized in Linsky and, if so, how the claims would be obvious. It is submitted that it would not be obvious to a person of ordinary skill in the art to modify Linsky et al. to arrive at the subject matter of claims 2-16 and 18-29. As has been pointed out above, claims 1 and 17 require storing a sequence of data samples contained in a time division multiplexed signal from a plurality of channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs, and outputting the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels with each data group containing a plurality of samples from

one of a plurality of channels and decoding the data samples with the sequence of data groups and outputting decoded data samples of the plurality of data groups from a plurality of channels. There is no basis for concluding that the mere utilization of time division multiplexing in the receiver of Linsky et al., would achieve the above subject matter of claims 2-16 and 18-29 except by impermissible hindsight.

The Examiner states that with respect to claims 9-12, Linsky shows a channelizer that he relies upon as being in Fig. 1 and further refers to satellite 212, of Fig. 2. In any event, Fig. 1 is described as a data chart that shows the processing of an information block 101 and an outer coded block 102. The Examiner's conclusion that the processing of Fig. 1 and further that the satellite 213 of Fig. 2 is a channelizer is traversed.

The channelizer in claims 9-12 is "responsive" to an input bandwidth which divides the input into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplex signal. The Examiner has admitted that time division multiplexing is <u>not</u> shown by Linsky et al. Therefore, it is <u>not</u> seen how Linsky et al. teach a channelizer when time division multiplexing is previously acknowledged by the Examiner not to be present in Linsky et al. and the channelizer is recited as producing an output channel comprising the time division multiplex signal. It is submitted that the Examiner is relying upon impermissible hindsight to allege that claims 9-12, which recite a channelizer, are obvious from Linsky *et al.* which does not even describe a channelizer. Claims 23-25, which also

recite a channelizer, are patentable for the same reasons noted regarding the patentability of claims 9-12.

In view of the foregoing amendments and remarks, it is submitted that each of the claims in the application is in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

Respectfully submitted,

Date: August 8, 2002

Noel F. Heal
Registration No. 26,074

TRW INC.
Intellectual Asset Management
One Space Park, E2/6051
Redondo Beach, CA 90278
Telephone: (310) 812-4910
FAX: (310) 812-2687

ATTACHMENT FOR SPECIFICATION AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/239,871; Filed: January 29, 1999

The following was substituted for the paragraph beginning on page 1, line 9:

Reference is made to related applications entitled "Serial to Parallel Conversion of Data to Facilitate Sharing a Single Buffer Among Multiple Channels," [",] filed on even date herewith as U.S. Serial No. 09/239,872 [(Attorney Docket No. 199.36692X00/TRW22-0072)]; and "Buffering and Sequencing of Data From Multiple Channels Through a Shared Decoder," [",] filed on even date herewith as U.S. Serial No. 09/240,171 [(Attorney Docket No. 199.36693X00/TRW22-0073)], which applications are incorporated herein by reference in their entirety.

The following was substituted for the paragraph beginning on page 3, line 8:

In each of the sub-band FDM modes discussed above, transmission may occur in one of two error correction modes which are, [i]heavy[i] or [i]light[i]. In both the heavy and light cases, an outer code is used for data encoding which is typically a Reed-Solomon code over GF (256) of size (236, 212). In the heavy case, an inner code is also used. This inner code is typically a short rate one-half block code as, for example, the (8,4) biorthogonal code.

The following was substituted for the paragraph beginning on page 5, line 23:

The phase lock loop provided by the phase tracking and preamble processing functions 20 and 22 operates in one of two modes relative to a decision direction depending upon whether the decoder and demodulator 10 is operating in the ZL or ZH modes. For light code bursts, the phase lock loop processes the {p(n)}, {q(n)} sample pairs for each symbol [as] independently and forms an error estimate for the

phase lock loop filter. In a typical case in the light mode, the phase lock loop is a first order phase lock loop which simply accumulates $k^*\varepsilon_n$ to yield the phase estimate θ wherein ε_n is the phase error estimate for each sample pair. Since synchronization for advanced satellites maintains the uplink frequency within a very tight tolerance which is typically no worse than ±500 Hz or equivalently, 0.001 revolution per symbol epoch for the slowest transmission data rate of typically 500 kilosymbols per second for the Z mode, a simple first order loop with a gain k in the range of 1/16 is adequate to track the phase. The demodulator and decoder may optionally use a lower loop gain when processing bursts from modes Y and X which have a higher symbol rate.

The following was substituted for the paragraph beginning on page 8, line 11:

A multichannel data demultiplexing and reordering memory processes the output data from multiple channels outputted from the phase tracking function. Time division multiplexed (TDM) [processors] processing of multiple channels eliminates parallel processing paths for each of the channels as in the prior art which required a soft and a hard decision processing path for each of the channels.

The following was substituted for the paragraph beginning on page 9, line 24:

A method of data reception in accordance with the invention includes receiving and storing a time division multiplexed signal containing a sequence of data samples from a plurality of channels; outputting the stored data samples in a sequence of data groups, each data group containing a plurality of samples from one of the plurality of channels; decoding the data samples within each data group; and outputting the

decoded data samples of the plurality of data groups. The data samples may each comprise orthogonally encoded data; and the decoder may be an inner code soft decision biorthogonal decoder. The orthogonally encoded data samples may be QPSK encoded. The data <u>in a preferred application</u> is received by a satellite. An input bandwidth is received and is divided with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed access signal. The data samples are stored in a memory comprising a write address generator and a record address generator and an addressable storage array containing memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells by addresses generated by the write address generator and the sequence of data groups are each individually read out from a group of memory cells by addresses generated by the read address generator.

The following was substituted for the paragraph beginning on page 12, line 20:

Fig. 3 illustrates the operation of the multiple channel data demultiplexing and reordering memory 114 which may be a RAM. The data is in accordance with a key of $Y_m(n)$ wherein m is the channel number and n is the time index. Therefore, it is seen, for example, that the sample Y1(1) is a data sample [form] <u>from</u> channel number one at time index one. As illustrated, the "INCOMING DATA" 202 is TDM samples 204 from channels Y1, Y2, Y3, Y4 and Y5. Each sample 204 is representative of two-bit symbols which are encoded by QPSK encoding and each are stored in a pair of memory cells. The data structure after storing the sequence of individual lines 202 of "INCOMING

DATA" is in the block 206 located to the right of the legend "WRITE INTO RAM". The block 206 is comprised of four rows 208 of data samples which are identical to the incoming data 202 and are sequentially read in columns from successive stored lines 202 of the block 206 of the stored TDM input data.

ATTACHMENT FOR CLAIM AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/239,871; Filed: January 29, 1999

1. A receiver comprising:

a memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal from a plurality <u>of</u> channels <u>with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs</u> and outputs the stored data samples in a sequence of data groups <u>equal in number to a number of the plurality of channels</u> with each data group containing a plurality of samples from one of the plurality of channels; and

a decoder, responsive to the <u>sequence of</u> data groups, which decodes the data samples within the sequence of data groups and outputs decoded data samples <u>of the plurality of data groups from the plurality of channels</u>.

17. A method of data reception comprising:

receiving and storing a time division multiplexed signal containing a sequence of data samples from a plurality of channels <u>with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs</u>;

outputting the stored data samples in a sequence of data groups <u>equal in number to a number of the plurality of channels</u>, each data group containing a plurality of samples from one of the plurality of channels;

decoding the data samples within [each] <u>the sequence of</u> data group<u>s</u>; and

outputting the decoded data samples of the plurality of data groups from the plurality of channels .

18. A method in accordance with claim [18] 17 wherein:

the data samples each comprise orthogonally encoded data; and

the decoder is an inner code soft decision biorthogonal decoder.

FIG. 3

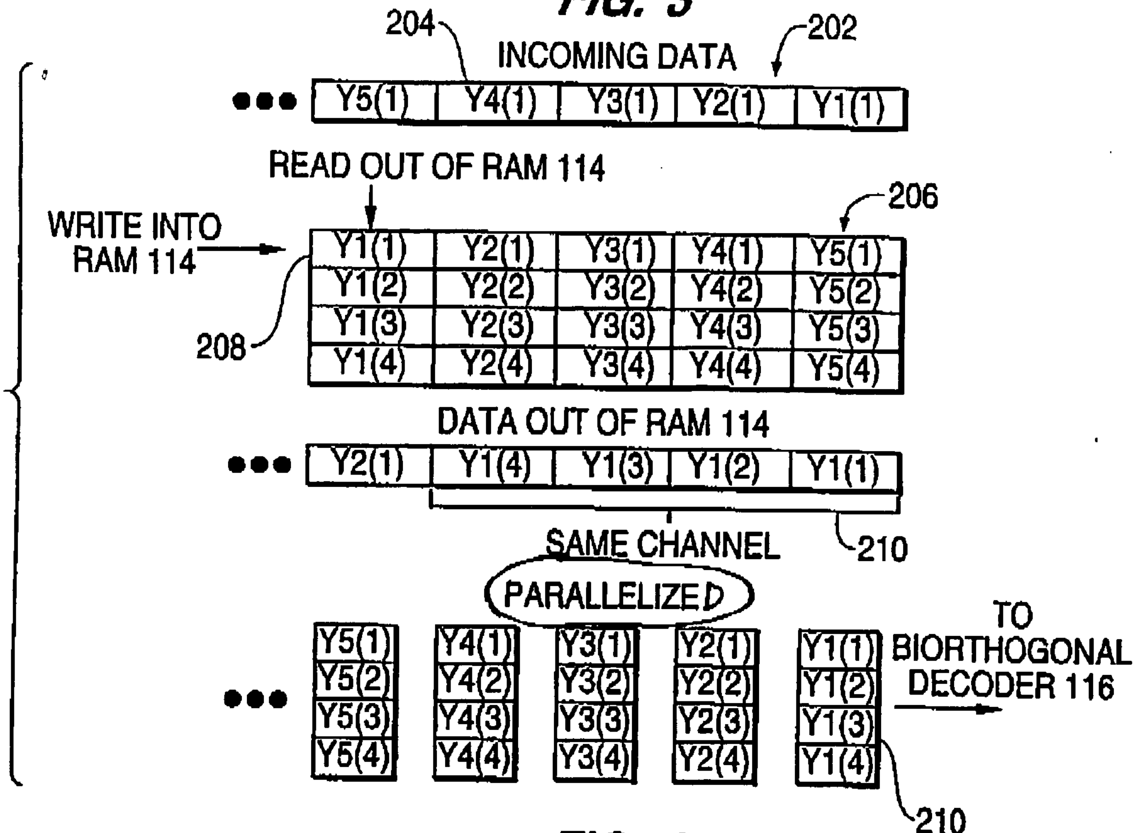
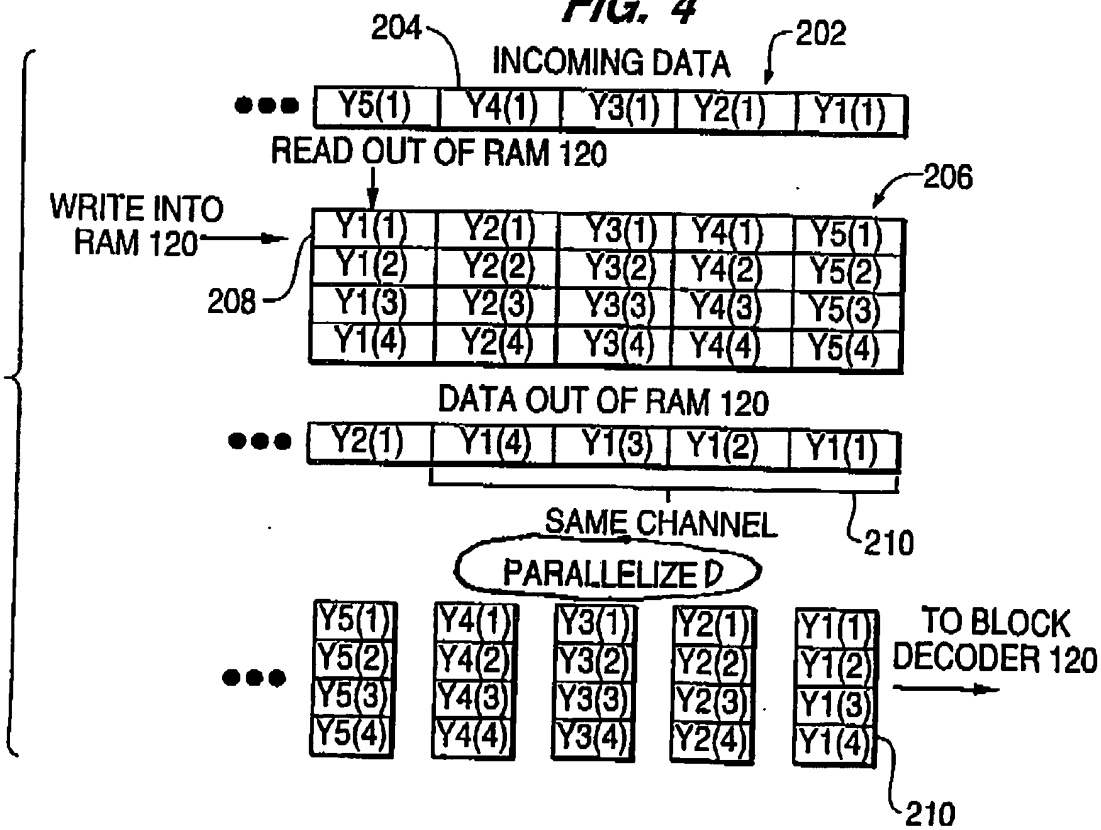

204
INCOMING DATA
202
Y5(1) Y4(1) Y3(1) Y2(1) Y1(1)
READ OUT OF RAM 114
206
WRITE INTO RAM 114
Y1(1) Y2(1) Y3(1) Y4(1) Y5(1)
Y1(2) Y2(2) Y3(2) Y4(2) Y5(2)
Y1(3) Y2(3) Y3(3) Y4(3) Y5(3)
Y1(4) Y2(4) Y3(4) Y4(4) Y5(4)
208
DATA OUT OF RAM 114
Y2(1) Y1(4) Y1(3) Y1(2) Y1(1)
SAME CHANNEL
210
PARALLELIZED
TO BIORTHOGONAL DECODER 116
210

FIG. 4


204
INCOMING DATA
202
Y5(1) Y4(1) Y3(1) Y2(1) Y1(1)
READ OUT OF RAM 120
206
WRITE INTO RAM 120
Y1(1) Y2(1) Y3(1) Y4(1) Y5(1)
Y1(2) Y2(2) Y3(2) Y4(2) Y5(2)
Y1(3) Y2(3) Y3(3) Y4(3) Y5(3)
Y1(4) Y2(4) Y3(4) Y4(4) Y5(4)
208
DATA OUT OF RAM 120
Y2(1) Y1(4) Y1(3) Y1(2) Y1(1)
SAME CHANNEL
210
PARALLELIZED
TO BLOCK DECODER 120
210